

Pipeline processor Report

Team 1



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| --- | --- |
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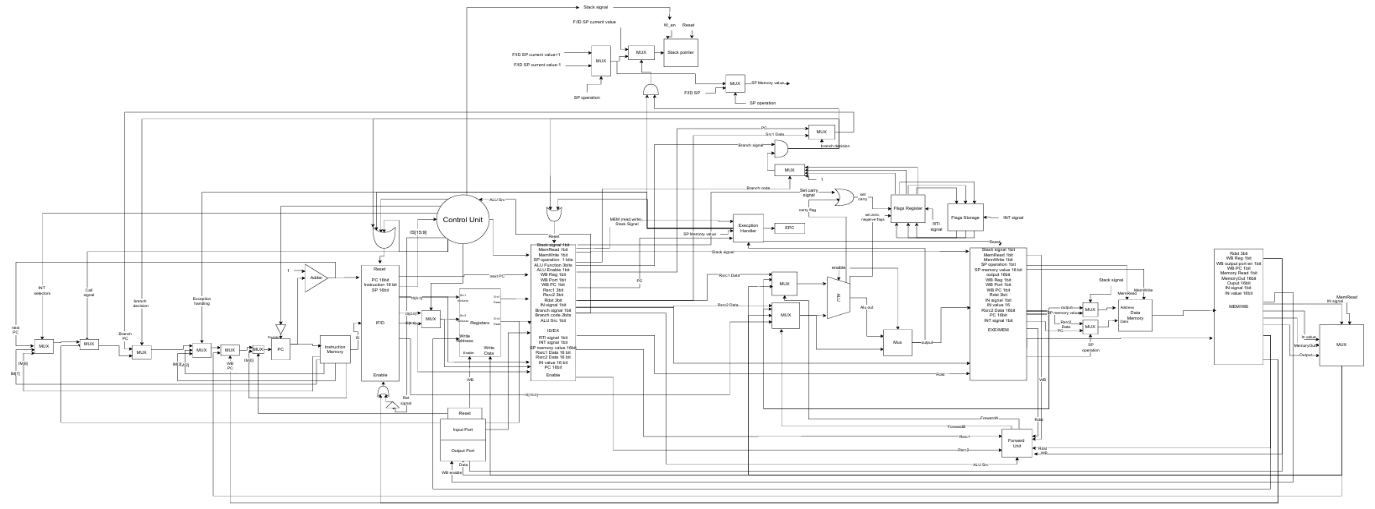
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# Instruction Format

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | First part of instruction | | | | Second part of instruction |
| Instruction | Opcode(7bits) | Rdst(3bits) | Rsrc1(3bits) | Rsrc2(3bits) | Immed(16bits) |
| NOP | 0000000 | Don’t care | Don’t care | Don’t care | Not Exist |
| SETC | 0000001 | Don’t care | Don’t care | Don’t care | Not Exist |
| MOV Rdst, Rsrc2 | 0000010 | Address from 0-7 | Don’t care | Address from 0-7 | Not Exist |
| NOT Rdst, Rsrc1 | 0000011 | Address from 0-7 | Address from 0-7 | Don’t care | Not Exist |
| AND Rdst, Rsrc1, Rsrc2 | 0000100 | Address from 0-7 | Address from 0-7 | Address from 0-7 | Not Exist |
| INC Rdst, Rsrc1 | 0000101 | Address from 0-7 | Address from 0-7 | Don’t care | Not Exist |
| ADD Rdst, Rsrc1, Rsrc2 | 0000110 | Address from 0-7 | Address from 0-7 | Address from 0-7 | Not Exist |
| SUB Rdst, Rsrc1, Rsrc2 | 0000111 | Address from 0-7 | Address from 0-7 | Address from 0-7 | Not Exist |
| IADD Rdst, Rsrc1, Imm | 0001000 | Address from 0-7 | Address from 0-7 | Don’t care | Exist |
| LDD Rdst, offset(Rsrc1) | 0001001 | Address from 0-7 | Address from 0-7 | Don’t care | Exist |
| STD Rsrc2, offset(Rsrc1) | 0001010 | Address from 0-7 | Address from 0-7 | Don’t care | Exist |
| LDM Rdst, Imm | 0001011 | Address from 0-7 | Don’t care | Don’t care | Exist |
| PUSH Rsrc2 | 0001100 | Don’t care | Don’t care | Address from 0-7 | Not Exist |
| POP Rdst | 0001101 | Address from 0-7 | Don’t care | Don’t care | Not Exist |
| CALL Rsrc2 | 0001110 | Don’t care | Don’t care | Address from 0-7 | Not Exist |
| RET | 0001111 | Don’t care | Don’t care | Don’t care | Not Exist |
| RTI | 0010000 | Don’t care | Don’t care | Don’t care | Not Exist |
| IN Rdst | 0010001 | Address from 0-7 | Don’t care | Don’t care | Not Exist |
| OUT Rsrc2 | 0010010 | Don’t care | Don’t care | Address from 0-7 | Not Exist |
| JZ Rsrc1 | 0010011 | Don’t care | Address from 0-7 | Don’t care | Not Exist |
| JN Rsrc1 | 0010100 | Don’t care | Address from 0-7 | Don’t care | Not Exist |
| JC Rsrc1 | 0010101 | Don’t care | Address from 0-7 | Don’t care | Not Exist |
| JMP Rsrc1 | 0010110 | Don’t care | Address from 0-7 | Don’t care | Not Exist |
| INT 0 | 0100000 | Don’t care | Don’t care | Don’t care | Not Exist |
| INT 2 | 1000000 | Don’t care | Don’t care | Don’t care | Not Exist |
| HLT | 1100000 | Don’t care | Don’t care | Don’t care | Not Exist |

# Schematic Design for the processor



# Pipeline stages design

## Pipeline registers details:

|  |  |
| --- | --- |
| Register | Size |
| Fetch/Decode | 48 bits |
| Decode/ Execute | 107 bits |
| Execute/Memory | 92 bits |
| Memory/Writeback | 56 bits |

## Pipeline hazards

We don’t have Data hazard.

We have a full forwarding unit that forwards data from Execute to Execute stage or from Memory to Execute stage

Branch Prediction: We use a static predictor (untaken)